CLAIMS

What is claimed is.

1. A phase-change memory device comprising:

spaced-apart first and third active areas that are disposed in a substrate;

a recess comprising a bottom and walls, wherein the recess communicates to the first active area and the third active area; and

a polysilicon film disposed in the recess, wherein the polysilicon film has a first conductivity at the bottom and a second conductivity at the walls.

2. The phase-change memory device according to claim 1, wherein the first and second active areas are spaced apart along a first symmetry line, further comprising:

a third active area that is spaced apart from the first active area along a second symmetry line that is orthogonal to the first symmetry line, wherein the polysilicon film is continuous between the first active area and the second active area.

3. The phase-change memory device according to claim 1, wherein the first and third active areas are spaced apart along a second symmetry line, further comprising:

a second active area that is spaced apart from the first active area along a first symmetry line that is orthogonal to the second symmetry line.

4. The phase-change memory device according to claim 1, further comprising:

a first isolation structure that is disposed in the substrate parallel to the second symmetry line.

5. The phase-change memory device according to claim 1, further comprising:

a first isolation structure that is disposed in the substrate parallel to the second symmetry line; and

a second isolation structure that is disposed in the substrate orthogonal to the first isolation structure.

6. The phase-change memory device according to claim 1, further comprising:

a first isolation structure that is disposed in the substrate parallel to the second symmetry line; and

a second isolation structure that is disposed in the substrate orthogonal to the first isolation structure, and wherein the first isolation structure comprises a discontinuous upper surface and the second isolation structure comprises a substantially continuous upper surface.

7. The phase-change memory device according to claim 1, wherein the first active area comprises a memory cell structure comprising:

a P+ Si structure disposed upon an N Si structure, wherein the P+ Si structure has a top and a bottom, wherein the N Si structure has a top and a bottom; and wherein the second isolation structure has a top and a bottom; and

wherein the second isolation structure bottom is below the P+ Si structure.

8. The phase-change memory device according to claim 1, wherein the first active area comprises a memory cell structure comprising:

a P+ Si structure disposed upon an N Si structure, wherein the P+ Si structure has a top and a bottom, wherein the N Si structure has a top and a bottom; and wherein the second isolation structure has a top and a bottom; and

wherein the second isolation trench bottom is below the P+ Si structure, and wherein the second isolation structure top is above the P+ Si structure bottom.

9. A memory device comprising:

in a substrate, a trench that exposes first, and second active areas along a first symmetry line and that exposes the first and a third active area along a second symmetry line that is orthogonal to the first symmetry line;

a polysilicon film disposed in the trench, wherein the polysilicon film contacts the first and third active areas; and

a phase-change memory element disposed above the first active area.

10. The memory device according to claim 9, further comprising:

a fourth active area;

and wherein the polysilicon film further comprises:

a first polysilicon film portion that is disposed between the first and third active areas; and

a second polysilicon film portion that is disposed between the second and fourth active areas.

11. The memory device according to claim 9, wherein the polysilicon film has a first conductivity between the first active area and the third active area, and a second conductivity superadjacent each active area.

12. The memory device according to claim 9, wherein the polysilicon film has a first conductivity between the first active area and the third active area, a second conductivity

superadjacent each active area, and the first conductivity between the first active area and the second active area.

13. The phase-change memory device according to claim 9, further comprising:

a first isolation structure that is disposed in the substrate parallel to the second symmetry line; and

a second isolation structure that is disposed in the substrate orthogonal to the first isolation structure.

14. A process of forming a phase-change memory device comprising:

forming a recess in a substrate, wherein the recess exposes spaced-apart first and third active areas, and wherein the recess comprises a bottom and walls;

forming a polysilicon film in the recess; and

treating the polysilicon film to have a first conductivity at the bottom and a second conductivity at the walls.

15. The process according to claim 14, wherein treating comprises:

first angled doping the polysilicon film that is in contact with the first active area; and

second angled doping the polysilicon film that is in contact with the second active area.

16. The process according to claim 14, wherein treating further comprises doping the polysilicon film to form discrete isolated regions of the second conductivity.

17. The process according to claim 14, before treating, further comprising:

forming a temporary material in the recess; and

patterning the temporary material to expose the polysilicon film that is directly above the active areas.

18. The process according to claim 14, before treating, further comprising:

forming a temporary material in the recess;

patterning a mask over the temporary material; and

removing a portion of the temporary material to expose the polysilicon film that is directly above the active areas.

19. The process according to claim 14, further comprising:

forming a first isolation trench in the substrate to define spaced-apart first and second areas; and

forming a second isolation trench adjacent the first and second areas to define a third area.

20. The process according to claim 19, further comprising:

treating the first and third areas to form the first and third active areas.

21. The process according to claim 19, wherein the second isolation trench is orthogonal to the first isolation trench.

22. The process according to claim 19, wherein the second isolation trench is shallower than the first isolation trench.

23. The process according to claim 19, after forming the first isolation trench, further comprising:

filling the first isolation trench with an isolation dielectric; and

planarizing the substrate.

24. The process according to claim 19, after forming the first isolation trench, further comprising:

forming a thermal dielectric film in the first isolation trench;

filling the first isolation trench with an isolation dielectric; and

planarizing the substrate.

25. The process according to claim 19, after forming the second isolation trench, further comprising:

filling the second isolation trench with an isolation dielectric; and

planarizing the substrate.

26. The process according to claim 19, after forming the second trench, further comprising:

forming a thermal dielectric film in the second isolation trench;

filling the second isolation trench with an isolation dielectric; and

planarizing the substrate.

27. The process according to claim 19, further comprising:

forming a diode stack that is contiguous to the first isolation trench and the second isolation trench;

filling the first isolation trench and the second isolation trench; and

forming a self-aligned silicide layer upon the diode stack.

28. A process comprising:

forming a trench in a semiconductor substrate, wherein the trench exposes two active areas that are situated along the transverse axis of the trench, and wherein the trench exposes at least two active areas that are situated along the longitudinal axis of the trench; and

forming a phase-change memory element above each active area.

29. The process according to claim 28, further comprising:

forming a polysilicon film in the recess; and

treating the polysilicon film to have a first conductivity at the bottom and a second conductivity at the walls.

30. The process according to claim 28, wherein treating comprises:

first angled doping the polysilicon film that is in contact with the first active area; and

second angled doping the polysilicon film that is in contact with the second active area.

31. The process according to claim 28, wherein treating further comprises doping the polysilicon film to form discrete isolated regions of the second conductivity.

32. The process according to claim 28, before treating, further comprising:

forming a temporary material in the recess; and

patterning the temporary material to expose the polysilicon film that is directly above the active areas.

33. The process according to claim 28, before treating, further comprising:

forming a temporary material in the recess;

patterning a mask over the temporary material; and

removing a portion of the temporary material to expose the polysilicon film that is directly above the active areas.

34. The process according to claim 28, further comprising:

forming a polysilicon film in the recess; and

treating the polysilicon film to have a first conductivity at the bottom and a second conductivity at the walls;

planarizing the substrate to form electrode material;

modifying a portion of the electrode material so that the electrode material comprises a first portion having a first thermal coefficient of resistivity and a second portion having a different second thermal coefficient of resistivity.